IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Merwin H. Alferness et al.
Serial No.	:	10/667,029
Filed	:	September 18, 2003
For	:	METHODS AND APPARATUS FOR ALLOCATING BANDWIDTH FOR A NETWORK PROCESSOR
Examiner	:	Tanh Q Nguyen
Group Art Unit	:	2182
Confirmation No.	:	9131
Customer No.	:	46628

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APPELLANTS' BRIEF

Dear Sir:

Appellants hereby appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner in the Final Office Action dated October 20, 2008.

REAL PARTY IN INTEREST

The present application is assigned to International Business Machines Corporation, New Orchard Road, Armonk, New York 10504.

RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known to the Appellants or to the Appellant's legal representative which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF THE CLAIMS

Claims 1-23 have been rejected and are on appeal.

STATUS OF AMENDMENTS

An Amendment after the Final Office Action (request for reconsideration) was filed on January 13, 2009. The request was considered as indicated by the Advisory Action mailed on January 16, 2009.

SUMMARY OF CLAIMED SUBJECT MATTER

CLAIM 1

Independent claim 1 is directed to a method of self-adjusting allocation of memory bandwidth in a network processor system. The method comprises determining an amount of memory bandwidth of a network processor used by a plurality of data types to transmit data through a plurality of active ports (e.g., operations 204 and 206 of FIG. 2 and as discussed on pages 6-7, lines 1-27 of the specification). The method further comprises determining an amount of memory bandwidth of the network processor used by each of the plurality of data types (e.g., operations 204 and 206 of FIG. 2 and as discussed on pages 6-7, lines 1-27 of the specification). The method further comprises dynamically adjusting an amount of memory bandwidth allocated to at least one of the plurality of data types based on the determinations (e.g., operation 210 of FIG. 2 and as discussed on pages 7-8, lines 28-5 of the specification).

CLAIM 12

Independent claim 12 is directed to an apparatus. The apparatus comprises port activation logic adapted to couple to a memory of a network processor (e.g., 114 and 104 of FIG. 1 and as discussed on pages 4-5, lines 31-27). The port activation logic is further adapted to interact with the memory so as to determine an amount of memory bandwidth of the network processor used by a plurality of data types to transmit data through a plurality of active ports (e.g., operations 204 and 206 of FIG. 2 and as discussed on pages 6-7, lines 1-27 of the specification). The port activation logic is further adapted to interact with the memory so as to determine an amount of memory bandwidth of the network processor used by each of the plurality of data types (e.g., operations 204 and 206 of FIG. 2 and as

discussed on pages 6-7, lines 1-27 of the specification). The port activation logic is further adapted to interact with the memory so as to dynamically adjust an amount of memory bandwidth allocated to at least one of the plurality of data types based on the determinations (e.g., operation 210 of FIG. 2 and as discussed on pages 7-8, lines 28-5 of the specification).

CLAIM 23

Independent claim 23 is directed to a network processor system. The network processor system comprises a memory (e.g., 104 of FIG. 1 and as discussed on pages 4-5, lines 19-27 of the specification). The network processor system further comprises a network processor coupled to the memory (e.g., 102 of FIG. 1 and as discussed on pages 4-5, lines 19-27 of the specification). The network processor comprises a memory controller (e.g., 108 of FIG. 1 and as discussed on pages 4-5, lines 19-27 of the specification). The network processor further comprises a plurality of ports (e.g., 106, 112 of FIG. 1 and as discussed on pages 4-5, lines 19-27 of the specification). The network processor further comprises port activation logic coupled to the memory controller and the plurality of ports and the memory (e.g., 114 of FIG. 1 and as discussed on pages 4-5, lines 19-27 of the specification). The port activation logic is adapted to interact with the memory so as to determine an amount of memory bandwidth of the network processor used by a plurality of data types to transmit data through a plurality of active ports (e.g., operations 204 and 206 of FIG. 2 and as discussed on pages 6-7, lines 1-27 of the specification). The port activation logic is further adapted to interact with the memory so as to determine an amount of memory

bandwidth of the network processor used by each of the plurality of data types (e.g., operations 204 and 206 of FIG. 2 and as discussed on pages 6-7, lines 1-27 of the specification). The port activation logic is further adapted to interact with the memory so as to dynamically adjust an amount of memory bandwidth allocated to at least one of the plurality of data types based on the determinations (e.g., operation 210 of FIG. 2 and as discussed on pages 7-8, lines 28-5 of the specification).

"MEANS" OR "STEP"

None of the claims contain an element expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-7, 11, 12-18, 22, and 23 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,098,123 to Olnowich [hereinafter *Olnowich*]. Claims 8-10 and 19-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Olnowich*.

ARGUMENT

REVIEW OF OLNOWICH

Olnowich is directed to "digital parallel processing systems, wherein a plurality of nodes communicate via messages over an interconnection network." *Olnowich,* col. 1, lines 9-11. Specifically, *Olnowich* "deals with the message store and forward

mechanism which operates between each processing node and the interconnection network." *Olnowich*, col. 1, lines 11-14. The citations to *Olnowich* discuss (1) the function of ports (send/receive), (2) the destination of data from ports (processor/network), and (3) the slowing of the transmission rate of ports. *Olnowich*, col. 1, lines 30-35, FIG. 5, col. 3, lines 51-66, and cols. 3-4, lines 62-2.

The citations to *Olnowich* fail to disclose, for example, determining an amount of memory bandwidth of a network processor used by a plurality of data types to transmit data through a plurality of active ports.

A PRIMA FACIE CASE OF ANTICIPATION OF CLAIMS 1-7, 11, 12-18, 22, AND 23 HAS NOT BEEN ESTABLISHED AS THE CITATIONS TO *OLNOWICH* FAIL TO DISCLOSE DETERMINING AN AMOUNT OF MEMORY BANDWIDTH OF A NETWORK PROCESSOR USED BY A PLURALITY OF DATA TYPES TO TRANSMIT DATA THROUGH A PLURALITY OF ACTIVE PORTS

Appellants respectfully submit that the record fails to establish that each feature of independent claims 1, 12, and 23 is disclosed by *Olnowich*. Accordingly, Appellants respectfully submit that the record fails to establish a prima facie case of anticipation.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *MPEP* § 2131, (8th Ed. 2001) (Rev. 7, July 2008) (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Id.* (citing *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236,

9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). Further, "[t]he elements must be arranged as required by the claim…" *Id.* (citing *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

> Independent claim 1 recites, inter alia
>
> determining an amount of memory bandwidth of a network processor used by a plurality of data types to transmit data through a plurality of active ports.

Independent claims 12 and 23, which each have their own scope, recite similar features.

Appellants respectfully submit that *Olnowich* has not been shown to disclose at least the above feature. Specifically, it is submitted that the citations to *Olnowich* fail to disclose determining an amount of memory bandwidth of a network processor **used by a plurality of data types**. Accordingly, Appellants respectfully submit that a prima facie case of anticipation has not been established.

At page 4, the present application notes that in the art,

> memory bandwidth may cause a delay in the transmission of data of certain data types from a first output port while it is retrieving data to be transmitted from a second output port. Because a delay (e.g., an underrun) in the transmission of data of a certain data type (e.g., Fast Ethernet or Gigabit Ethernet, etc.) from the output ports corrupts the data, improved methods and apparatus for allocating memory bandwidth to avoid such delays or underruns are desired.

The present application then notes that "[m]ethods and apparatus for allocating memory bandwidth to avoid delays or underruns

while transmitting data of one or more data types are described [in the application]." *Id.* With regard to data types, the present application notes by way of inclusion that "[t]he data may be of one or more data types, such as ATM, Fast Ethernet, and/or Gigabit Ethernet." *Id.*

In contrast to these specifically addressed data types, the Office Action points to four (4) ports discussed in the cited passages of *Olnowich* for disclosing four different types of data. Specifically, the Office Action contends:

> port A and port B are used to transmit data to and from processor 4; port C and port D are used to transmit data to and from network 2 - hence four different data types through ports A, B, C, D (col. 1, lines 30-36; FIG. 5)

Additionally, the Advisory Action points to data being slowed from one speed to another speed. However, neither the function of a port (send/receive), the destination of its data (processor/network), nor the slowing of the transmission speed of data have been shown by the Office to equate to "a plurality of data **types**." That is, these passages have not been shown to disclose anything other than one type of data being transmitted using four (4) different ports.

Appellants respectfully note that the burden is on the Office, **not the Appellant**, to establish a prima face case. In this instance, the burden is on the Office to establish that ports A-D transmit more than one type of data. Appellants respectfully submit that the Office has not yet met this burden.

In view of the above, Appellants respectfully submit that *Olnowich* cannot properly be relied upon for disclosing the above feature. Further, it is again noted that the above

feature is an expressly recited feature in the claims. Accordingly, favorable review and reversal of the rejection under 35 U.S.C. § 102 are respectfully requested.

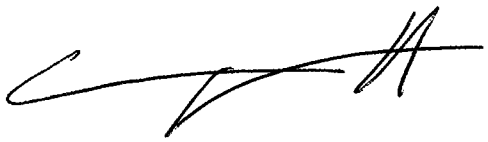
A PRIMA FACIE CASE OF OBVIOUSNESS OF CLAIMS 8-10 AND 19-21 HAS NOT BEEN ESTABLISHED AS NO SECONDARY CITATION IS OFFERED THAT WOULD REMEDY THE ABOVE DEFICIENCY OF THE REJECTION OF THE INDEPENDENT CLAIMS

Claims 8-10 and 19-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Olnowich*. As discussed above, the cited passages of *Olnowich* fail to disclose all of the features recited in independent claims 1 and 12, from which claims 8-10 and 19-21 ultimately depend. No secondary citation is offered that would cure this deficiency. Accordingly, Appellants respectfully submit that claims 8-10 and 19-21 are allowable for at least the reasons given in support of independent claims 1 and 12.

CONCLUSION

Appellants do not believe any other fees are due regarding this Brief. However, if any additional fees are required, please charge deposit account no. 04-1696.

Respectfully Submitted,



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Dated: June 15, 2009
Hawthorne, New York

CLAIM APPENDIX

The following claims are under appeal:

Claim 1 (Previously Presented): A method of self-adjusting allocation of memory bandwidth in a network processor system comprising:

determining an amount of memory bandwidth of a network processor used by a plurality of data types to transmit data through a plurality of active ports;

determining an amount of memory bandwidth of the network processor used by each of the plurality of data types; and

dynamically adjusting an amount of memory bandwidth allocated to at least one of the plurality of data types based on the determinations.

Claim 2 (Original): The method of claim 1 wherein a total amount of memory bandwidth of the network processor used by the plurality of data types is configurable.

Claim 3 (Original): The method of claim 2 further comprising determining whether memory bandwidth may be allocated to at least one of the plurality of data types.

Claim 4 (Previously Presented): The method of claim 3 wherein determining whether memory bandwidth may be allocated to at least one of the plurality of data types includes determining a difference between a maximum amount of memory bandwidth of the network processor that may be used by the plurality of data

types and a total amount of memory bandwidth of the network processor currently used by the plurality of data types.

Claim 5 (Original): The method of claim 3 wherein determining whether memory bandwidth may be allocated to at least one of the plurality of data types includes determining whether a port for transmitting data of at least one of the plurality data types may be activated.

Claim 6 (Previously Presented): The method of claim 1 wherein determining an amount of memory bandwidth of the network processor used by each of a plurality of data types includes:

determining a number of active ports of the network processor used to transmit data of each of the plurality of data types; and

determining an amount of memory bandwidth allocated to each active port for each of the plurality of data types.

Claim 7 (Original): The method of claim 6 wherein the amount of memory bandwidth allocated to each active port for a data type is the same.

Claim 8 (Original): The method of claim 6 wherein the amount of memory bandwidth allocated to each active port for an ATM protocol data type is configurable.

Claim 9 (Original): The method of claim 1 wherein the plurality of data types includes at least one of an ATM protocol data type and an Ethernet protocol data type.

Claim 10 (Original): The method of claim 9 wherein the Ethernet protocol data type includes at least one of a Gigabit Ethernet data type and a Fast Ethernet data type.

Claim 11 (Previously Presented): The method of claim 1 wherein dynamically adjusting the amount of memory bandwidth allocated to at least one of the plurality of data types based on the determinations includes at least one of dynamically activating and deactivating a port for transmitting data of at least one of the plurality of data types.

Claim 12 (Previously Presented): An apparatus comprising:

port activation logic, adapted to couple to a memory of a network processor and to interact with the memory so as to:

determine an amount of memory bandwidth of the network processor used by a plurality of data types to transmit data through a plurality of active ports;

determine an amount of memory bandwidth of the network processor used by each of the plurality of data types; and

dynamically adjust an amount of memory bandwidth allocated to at least one of the plurality of data types based on the determinations.

Claim 13 (Original): The apparatus of claim 12 wherein a total amount of memory bandwidth of the network processor used by the plurality of data types is configurable.

Claim 14 (Original): The apparatus of claim 13 wherein the port activation logic is further adapted to determine whether memory bandwidth may be allocated to at least one of the plurality of data types.

Claim 15 (Previously Presented): The apparatus of claim 14 wherein the port activation logic is further adapted to determine a difference between a maximum amount of memory bandwidth of the network processor that may be used by the plurality of data types and a total amount of memory bandwidth of the network processor currently used by the plurality of data types.

Claim 16 (Original): The apparatus of claim 14 wherein the port activation logic is further adapted to determine whether a port for transmitting data of at least one of the plurality data types may be activated.

Claim 17 (Original): The apparatus of claim 12 wherein the port activation logic is further adapted to:

determine a number of active ports of the network processor used to transmit data of each of the plurality of data types; and

determine an amount of memory bandwidth allocated to each active port for each of the plurality of data types.

Claim 18 (Original): The apparatus of claim 17 wherein the amount of memory bandwidth allocated to each active port for a data type is the same.

Claim 19 (Original): The apparatus of claim 17 wherein the amount of memory bandwidth allocated to each active port for an ATM protocol data type is configurable.

Claim 20 (Original): The apparatus of claim 12 wherein the plurality of data types includes at least one of an ATM protocol data type and an Ethernet protocol data type.

Claim 21 (Original): The apparatus of claim 20 wherein the Ethernet protocol data type includes at least one of a Gigabit Ethernet data type and a Fast Ethernet data type.

Claim 22 (Original): The apparatus of claim 12 wherein the port activation logic is further adapted to at least one of dynamically activate and deactivate a port for transmitting data of at least one of the plurality of data types.

Claim 23 (Previously Presented): A network processor system comprising:

a memory; and

a network processor coupled to the memory, the network processor comprising:

a memory controller;

a plurality of ports; and

port activation logic, coupled to the memory controller, the plurality of ports and the memory, and adapted to interact with the memory so as to:

determine an amount of memory bandwidth of the network processor used by a plurality of data types to transmit data through a plurality of active ports;

determine an amount of memory bandwidth of the network processor used by each of the plurality of data types; and

dynamically adjust an amount of memory bandwidth allocated to at least one of the plurality of data types based on the determinations.

EVIDENCE APPENDIX

Not applicable

RELATED PROCEEDINGS APPENDIX

Not applicable